EE / CPRE / SE 491 - sdmay20-38
iFPGA - Intermittent Intelligent FPGA Platform
Week7 Report

1/30/20 - 2/13/20
Client: Henry Duwe
Faculty Advisor: Henry Duwe

Team Members:

Jake Tener - Team member, SW focus
Jake Meiss - Team member, HW focus
Andrew Vogler - Team member, FPGA focus
Zixuan Guo - Team member, FPGA focus
Justin Sung - Team member, FPGA focus

Weekly Summary

- The goal of this week was to establish communications between the MSP430 and the IGLOO nano via SPI protocol. Flash a program on both to be able to transfer data and access the RAM on the NANO.
- Solidify the hardware components to be bought for the PCB.
- Modify Aquila C++ libraries for sound recognition to be ported onto the MSP
- Make a prototype for the MAC accelerator on FPGA.

Past Week Accomplishments

- FPGA - Zixuan Guo
    - Use the systolic array as the algorithm to build the matrix multiplication.
    - Figured out how to read from SRAM in sequence(Use counter logic component).

- PCB Design - Jake Meiss
    - Finalization of the parts list for PCB implementation
    - Design schematic symbols and package footprints for the main integrated circuits being used

- SW - Jake Tener
    - Creation of testing programs that will analyze .wav files
    - Getting specific port mappings between MSP430 and Igloo Nano as well as code examples
    - Explored the Aquila libraries and generated an MFCC to be compared against Liberosa generation.

- HW - Justin Sung, Andrew Vogler
    - Tested the NANO and MSP connection over SPI

Pending Issues

- The SPI connection with the NANO and MSP did not work as expected, still trying to fix it.
- C library being used may not work as we think. That may or may not be a problem. TBD. Explore other C/C++ libraries able to handle MFCC generation
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Individual Contributions

Team Member	**Contribution**	**Weekly Hours**	**Total Hours**
Jake Tener	SW	8	20
Jake Meiss	PCB Design	6	20
Andrew Vogler	PCB Design	8	20
Zixuan Guo	FPGA	6	20
Justin Sung	SW	8	20

Plans for Coming Week

- Establish SPI communications
    - Be able to write data from MSP to NANO memory
    - Be able to write data from NANO to MSP
- Multiply-And-Accumulate
    - Continue progress
    - Synthesis VHDL program on the FPGA and read the data from SRAM
- Electrical Design
    - Finish up choosing external components
    - Start to design the prototype circuit for the power side and keep searching on FGPA and MSP schematic design.
- Software
    - Finish C program that will generate MFCC coefficients for a .wav file